Separation of a Silicon Substrate into Chips by Liquid Etching

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***Abstract*— In this paper we present a technological route for separating a silicon wafer into chips(crystals). The chip includes a MEMS membrane ($Si/SiO_2/Si_3N_4$) of various diameters (1.0 ÷ 2.4 mm) and has of square shape with a side of 6 mm. The relief of the structure was measured by a non-contact optical profilometer. The horizontal dimensions of the structure were determined by means of a microscope. The etching rate of silicon in plasma (SF_6/C_4F_8), a gas (F_2) and a liquid (12% KOH) was determined experimentally. The cassette (apparatus) for separation of wafers on chips was designed and manufactured. This new cassette makes it possible to increase the yield of silicon wafers by dividing them into chips without mechanical contact by replacing cutting tool on a liquid etchant. Also, process cutting by liquid etching reduces energy consumption. New cassette reduces probability of operator error and allows to form chips of various shape.**

Keywords*— *separation technology; cutting tools; cassette for etching; etching rate; silicon crystal; silicon chip

I. INTRODUCTION

Silicon wafers are using in processes of manufacturing devices in microelectronics. Repeated areas of wafer - chips are formed through lithography, deposition and etching of layers, etc. Separation of the final structure on the wafer into chips is final step of the technological route. Such wafers have the maximum cost since all technological operations (steps) have carried out, except for the separation into chips. Therefore it is extremely important to obtain the maximum yield of chips from each wafer. The probability of chip breakage during separation increases several times when the chip is a MEMS structure that is, the structure in which a part of the material (for example, a deposited film) is not on a wafer [1].

Different approaches exist to separate the wafers into chips. One of the basic methods is wafer separation by diamond tool [2-4]. During this process mechanical stresses are introduced, which appear as cracks. The degree of deformation of the chip structure depends on the scribing process parameters. In work [2] a special liquid was used in the process of diamond cutting to minimize mechanical stresses in the chip structure. The liquid reduces the strength of the silicon from 8.80 to 7.32 GPa. Another way of dividing wafers into chips is by using the sacrificial layer and ultrasound [5]. At present, the use of short-wave laser pulses is one of the non-contact scribing methods [6-9]. Using a laser increases the accuracy of the cut and reduces the roughness, which is important in view of the effect of scaling elements according to Moore's law [6]. In some cases, the laser does not make holes through the entire structure. The incisions have form of an ellipse, and it is a concentrator of mechanical stresses. The orientation of the ellipses determines the separation region. Tensile stresses are concentrated at the top of the ellipse. The resulting surface has a higher quality and strength than the surfaces cut using laser methods for cutting a bulk body, since the crystal form is preserved [7]. In work [8], during scribing process the angle of the walls is different from 90˚, which improves the parameters of the devices on the chips.

This work was carried out on the equipment of the R&D center "MST and ECB" and supported by Ministry of Education and Science of Russian Federation (within the agreement № 14.594.21.0012, id RFMEFI59417X0012).

II. THE CASSETTE FOR SEPARATING A SILICON WAFERS INTO CHIPS BY LIQUID ETCHING

The cassette (apparatus) for liquid etching was developed and manufactured (Fig.1) [1]. The construction of this cassette has several advantages over existing ones [10].

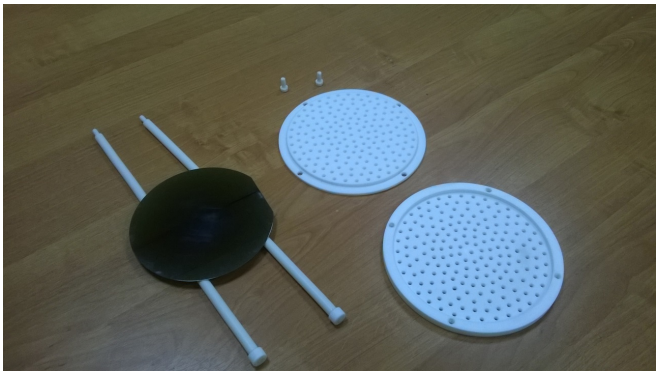

Fig. 1. The cassette for separating a silicon substrate on crystals by liquid etching.

The construction cassette for chemical separation of silicon wafers on chips is easier to manufacture. Simplicity of construction and ergonomics reduce the probability of operator error during the work of the proposed cassette. In the proposed cassette, the separation of the silicon wafer into

 978-1-5386-4340-2/18/$31.00©2018 IEEE

chips occurs without mechanical contact between the cutting tool and the shared structure due to the replacement of the cutting tool with a liquid etchant. This provides an increase in the yield of chips. It is possible to work both with the whole silicon wafer, and with its separate parts due to the use of a removable set of masks. Each mask contains a set of grooves for work, both with wafer, and with parts of wafer. The chips of an arbitrary shape are formed by changing the distance between the grooves of the masks.

Masks create a tight contact with the sample, closing the local area, which is not subject to etching. The chips are not displaced after the etching process. Fixation of the cassette part is carried out by means of threaded connections: bolt-cover-base and handle-cover-base. The cassette is transported by means of two handles. The length of the handles is selected depending on the depth of the bath for liquid etching. This cassette allows separating the wafers into chips without the use of electricity, which reduces the cost of the final operation and the development of a semiconductor device as a whole.

The proposed cassette construction provides a through flow of liquid etchant and water, due to the areas of perforation in the cover and in the base. Thus, the etching speed is stabilized during the material removal process and the etching uniformity is increased. This allows removing the entire etchant and avoiding removing the unplanned part of the wafer material. The near-surface layer with a high concentration of undesirable impurity is formed at the bottom of the deep bath during etching process. The use of the cassette feet raises the base above the bottom of the bath, which provides protection against ingress of unwanted impurities, improves the stability of the etching process, and also does not interfere with the circulation of the solution in the bath.

The cassette is used as follows. Cassette material is fluoroplastic, which does not react with the etchant. The silicon wafer is placed on a perforated base with legs, fixing with a removable set of masks. The perforated cover fixes the wafer. The cover is connected to the base by means of threaded connections of bolts and handles. The cassette is lowered into a bath of etchant. The etchant enters the working container of the cassette. The fluid reacts with the sample in the cavities through a perforated base and a perforated cover. The cassette rises from a bath with an etchant after the process is complete. Next, the cassette is placed in a bath with a deionized water to remove residual etchant. After that, the cassette rises from the bath with deionized water. The next step is drying. The cassette is unwound on a centrifuge in an atmosphere of an inert gas, for example nitrogen. The final step is to unscrew the bolts and handles, open the perforated cover and transfer wafer or chips in the case of splitting the wafer into parts with tweezers.

III. EXPERIMENT

We used silicon wafer with thickness 690 microns. A layer of thermal silicon oxide 0.6 um thick and thermal silicon nitride 0.13 um was formed on the wafer surface. One photolithography mask was used to form round membranes and regions with low mechanical strength. A layer of aluminum with a thickness of 0.9 um was used to protect wafer reverse side. Next, a technological route is presented (Fig.2).

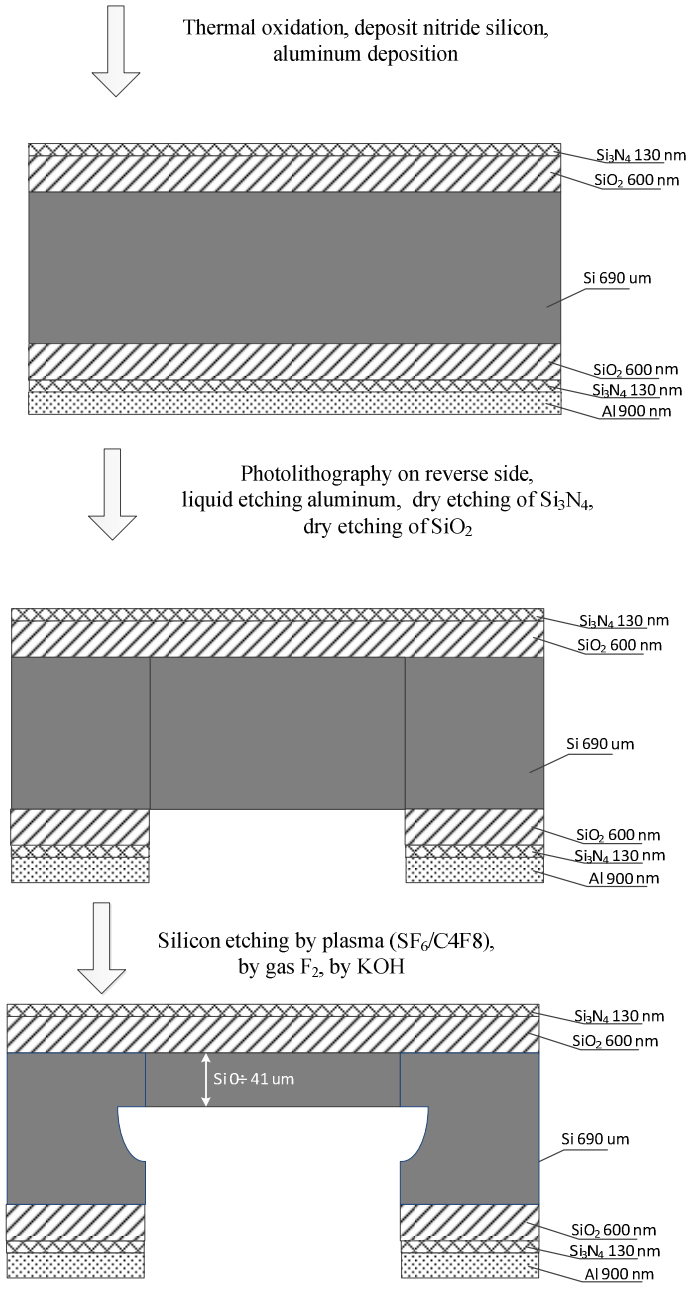

Fig.2. Technological route.

The use of thick aluminum layer allows eliminating the influence of the roughness of the reverse side of the wafer surface. Then, photolithography was carried out from reverse side. After that, vertical plasma chemical etching silicon was performed using alternating gases SF_6/C_4F_8 (Bosch process) to a depth of 460 um for 46 min. The general view of the wafer with obtained structures is shown below (Fig. 3).

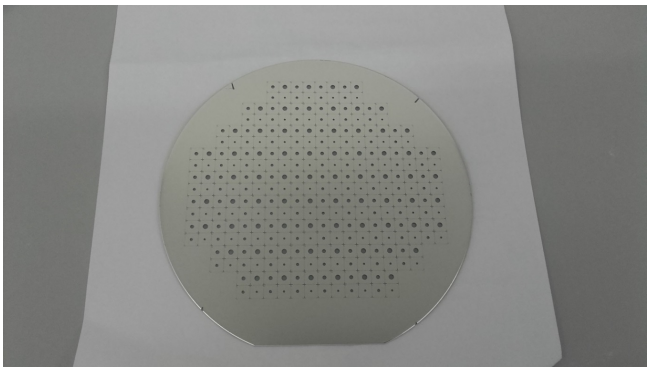

Fig. 3. General view of the wafer with obtained structures.

The horizontal dimensions and relief of the obtaining structures were determined by means of a microscope and a profilometer after each silicon etching step. The results in the three-dimensional form of the relief measurement by means of a non-contact optical profilometer are presented below (Fig. 4).

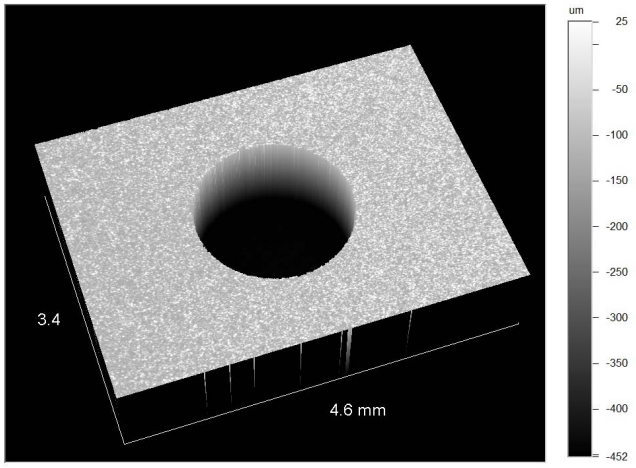

Fig.4. 3D surface relief after Bosch process.

The next step was etching in a F_2 gas on deep 81 um for 15 min. Then, re-etching silicon in a F_2 gas on deep 88 um. After that, the aluminum layer was removed by a liquid method. A repeated measurement of the horizontal dimensions was carried out (Fig. 5).

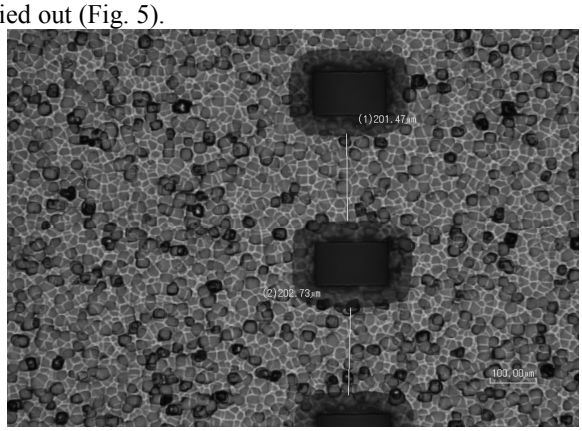

Fig. 5. Measuring the distance between perforated areas.

The initial gap between the perforation regions was 300 um. Thus, etching silicon in F_2 gas on deep at 169 um corresponds to 100 um in the variation of the horizontal gaps. Given that the closure occurs on both sides, we can conclude that (in gas F_2) $V_{etching.vert.} \approx 3.38 \times V_{etching.gor.}$ and $V_{etching.gor.}=1.6$ um/min.

The next step was etching silicon in 12% KOH solution for 5 hours under temperature 95 °C in the manufactured cassette. It is noticeable that the distance between the areas with perforation was reduced (Fig. 6).

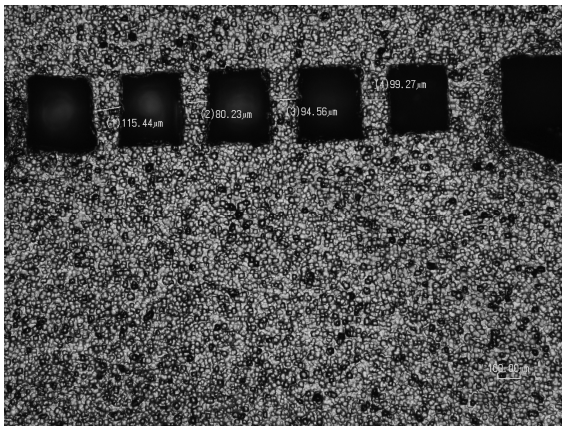

Fig.6. Perforated areas after liquid etching of silicon.

The average distance between the perforated areas is 100 um. This means that the horizontal etching rate of Si in KOH was 10 um/h. Figure 7 shows the surface relief after each etching step.

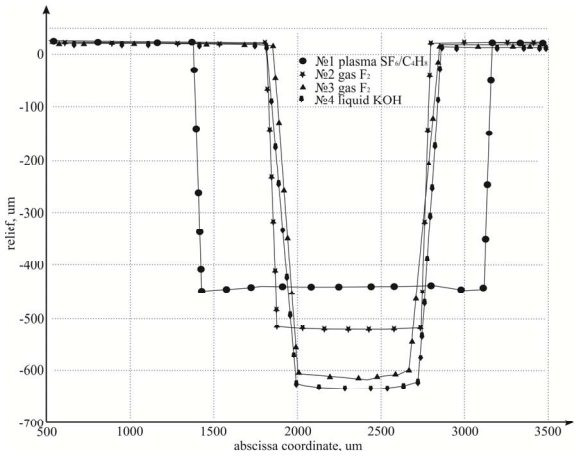

Fig.7. The surface relief after each etching step.

Figure 7 shows the results of silicon plasma chemical etching in SF_6/C_4F_8 for a membrane diameter of 1.8 mm. In the remaining cases, a diameter of 1.0 mm was analyzed. The change in the relief after etching in KOH was 15 um, hence the vertical etching rate was 3 um/h.

Using a scanning electron microscope, the thickness of the membrane materials was determined. The total thickness of the dielectric layers was 0.7 um. The thickness of silicon in the region of the membrane was 41 um (Fig. 8).

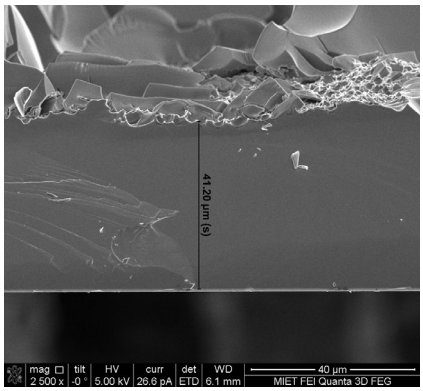

Fig. 8. Determination of thickness of silicon in region of the membrane.

The final liquid etching of silicon allowed the wafer to be divided into chips without use of mechanical contact (Fig.9).

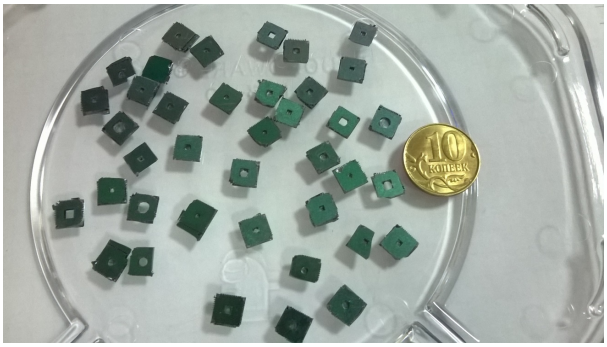

Fig. 9. View of the sample after the silicon wafer final etching.

The image of the chip with membrane after completion of all operations is shown below (Fig. 10). It can be seen that the diameter of the membrane was 1.44 mm.

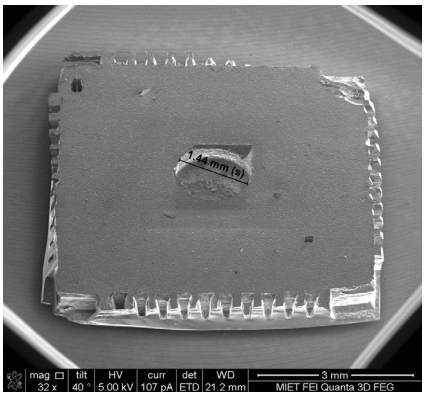

Fig. 10. The image of the chip with membrane after completion of all technological steps.

IV. Conclusions

In this paper, a technological route was presented that allows to form a set of chips of different geometry from a silicon wafer with a different set of dielectric layers. The cassette for non-contact separation silicon wafer into chips was demonstrated. Chips of a square shape with a side of 6 mm were made. The vertical etching rate of silicon in the Bosch process was 10 um/min. The vertical etching rate of silicon in the F_2 gas was 5.4 um/min, the horizontal velocity was 1.6 um/min. The vertical etching rate of silicon was 3 um/h in 12% KOH at a temperature of 95°C, the horizontal etch rate was 10 um/h.

Acknowledgment

This work was carried out on the equipment of the R&D center "MST and ECB" and supported by Ministry of Education and Science of Russian Federation (within the agreement № 14.594.21.0012, id RFMEFI59417X0012).

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